3D Photonic integration platform based on multilayer PolyBoard and TriPleX technology for optical switching and remote sensing and ranging applications

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Methodology for the experimental evaluation of 3PEAT modules and preparation of system test beds

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Executive Summary

The present document reports on the definition of testing procedures and performance evaluation scenarios for all 3PEAT modules. The first part of the report concerns the 3PEAT switching technology, the second the 3PEAT LDV technology.

Keywords: photonic integration, optical switching, laser Doppler vibrometry, TriPleX, PolyBoard.

List of Acronyms

ALC	Amplitude level control
AWGR	Arrayed waveguide grating router
BER	Bit error rate
CW	Continuous wave
DC	Direct current
DCN	Data center network
DFB	Distributed feedback laser
DSP	Digital signal processing
DUI	Device under test
EDFA	Erbium doped fiber amplifier
EO	Electro optic
FPGA	Field programmable gate array
IR	Infrared
KPI	Key performance indicator
LDV	Laser Doppler Vibrometry
LMS	Least mean square
LPF	Low pass filter
MZM	Mach-Zehnder modulator
NIC	Network interface card
OBPF	Optical bandpass filter

OPA	Optical phased array
OSA	Optical spectrum analyser
PC	Polarization controller
PD	Photodiode
PDL	Polarization dependent loss
PIC	Photonic integrated circuit
PPG	Pulse pattern generator
PRBS	Pseudo random binary sequence
TTL	Transistor-transistor logic
VOA	Variable optical attenuator
WP	Workpackage

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1. Introduction

In order to reveal the disruptive potential of the integrated hybrid TriPleX-Polyboard platform technology developed during 3PEAT, a sound performance evaluation of the individual building blocks and the interaction of them in form of modules is of uttermost importance. Only suitable testing methodologies and evaluation scenarios will allow a meaningful comparison to state of the art technology (e.g. bulk or fiber optics) and reveal the future prospects for commercialization. Thus, besides technology development another major task of WP6 of the 3PEAT project is to define appropriate system testbeds and their complementary evaluation criteria. Furthermore, also the necessary hardware setups (electronics and optics) for the lab based system testbeds, as well as for application near assessments need to be developed. The following report will summarize the corresponding and ongoing work of the 3PEAT consortium in this field. In accordance to the targeted application areas of the project, the report is subdivided into the 3PEAT switching (targeted modules 1 to 3) and the LDV technology (targeted modules 4 to 6).

2. Definition of testing procedures and performance evaluation scenarios

Within WP2 of the 3PEAT project, the manufacturers of switching and LDV technology already defined the system requirements and component specs for the targeted modules. The switching modules 1 and 2 will allow a sound examination of the basic components needed for switching technology. Module 3 will have a complex topology enabling application near tests and comparisons to state of the art switching technology. The situation is comparable for LDV technology. While module 4 will allow basic evaluation tests of individual parts of the hybrid technology platform, it is planned that module 5 and 6 will be operated under application near conditions. The LDV-demonstrator in form of module 6 will be equipped with an optical phased array (OPA) for integrated beam scanning.

2.1 3PEAT switching technology

2.1.1 Definition of testing methodologies

Within the framework of 3PEAT, novel optical switches for the intra-data center connectivity have been conceptualized, leveraging the advantages, on the one hand the low loss TriPleX platform and on the other hand, the multi-layer PolyBoard platform. More importantly, the two powerful photonic platforms will be combined by means of 3D integration techniques, minimizing the footprint of the devices. To this end, 3PEAT will

deliver two active optical switches (Module-1 and Module-3) based on an array of Mach-Zehnder interferometers equipped with PZT actuators in both arms, and on arrayed waveguide grating (AWG) and one passive optical switch, emulating an arrayed waveguide grating router (AWGR).

Testing procedures are defined to ensure coherence of results across different evaluation activities within WP6 as well as among the participating partners. The testing procedures will be executed to ensure that the specifications of the 3PEAT devices, defined in WP2, are met.

2.1.1.1 3PEAT Key Performance indicators

Testing of the 3PEAT optical switches will be carried out against the following **Key Performance Indicators** (KPIs), targeting the switches as individual components as well as network elements:

Insertion loss is the excess attenuation experienced by the optical signal during propagation in the optical switch. Insertion loss can be broken down primarily to propagation loss at the waveguides due to scattering and absorption as well as to coupling loss at the interfaces (fiber to PIC as well as polymer to silicon nitride) due to mode mismatch and reflection at the facets. Fiber to fiber loss will be measured for the 3PEAT optical switches, which is specified as $IL = 10\log_{10}\frac{P_{in}}{P_{out}}$ (in dB). Loss uniformity will be also calculated by measuring the insertion loss for all different input-output permutations of the switch.

Reconfiguration time is the time required for a reconfigurable component in order to change its state. The switching speed is assessed by measuring the instantaneous signal intensity at one or two ports of the device under test (e.g. with a photodetector connected to an oscilloscope) and is typically given as a percentage of the power levels at the initial and the final states, e.g. the 10-90 switching time is defined as the time it takes for the signal intensity to move from 10% to 90% of the steady state. Various definitions of the switching speed are used (5-95, 10-90, 80-20, 1/e) according to the purpose and context of the measurement. In 3PEAT, the 10-90 definition will be used for evaluating the switching time of the components.

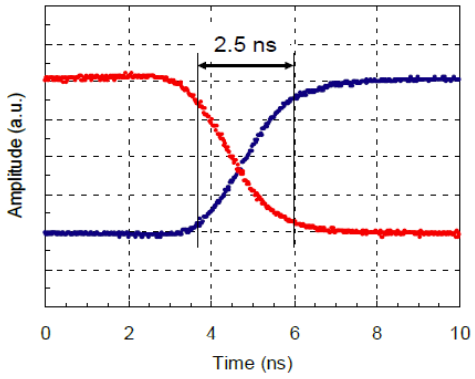

Figure 1: Switching time (10-90) measurement of an optical switch.

Reconfiguration time of devices that perform switching in the space domain like 3PEAT Module-1 and Module-3 can be measured directly by connecting a CW source and monitoring the signal intensity at one output port by means of a photodetector. In the case of the wavelength switch (Module-2), however, the measurement will be based on the combination of the passive wavelength switch with a fast-tunable laser, where the switching speed will be essentially defined by the wavelength tuning speed of the laser.

Polarization dependent loss (PDL) is the peak-to-peak difference in the insertion loss of an optical component or system with respect to all possible states of polarization. It is expressed as the difference between the maximum and minimum insertion loss in decibels when the polarization of the input signal is varied $PDL = IL_{max} - IL_{min}$.

Bit Error Rate (BER) is the number of bit errors per unit time. It can be formulated mathematically as $BER = p(1)P(0|1) + p(0)P(1|0)$ with reference to the terminology defined in Figure 2. For Gaussian noise, the BER is given by $BER = \frac{1}{4}\left[erfc\left(\frac{\mu_1 - y_d}{\sqrt{2}\sigma_1}\right) + erfc\left(\frac{y_d - \mu_0}{\sqrt{2}\sigma_0}\right)\right]$.

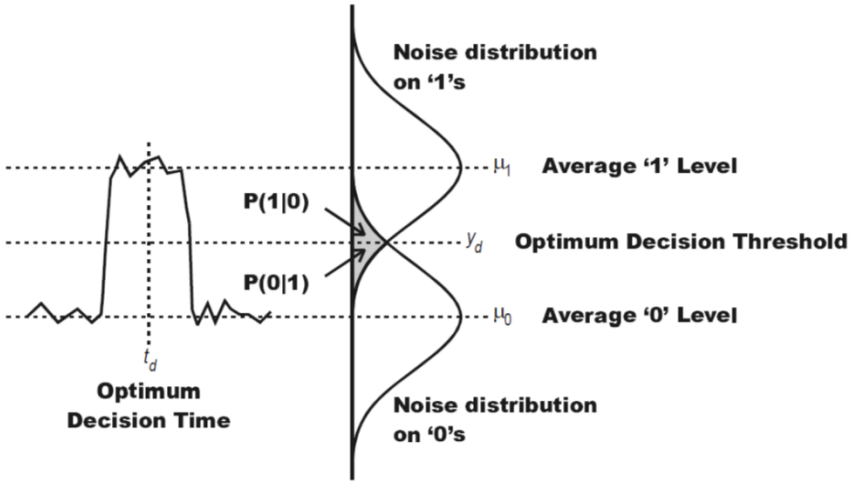

Figure 2: Gaussian noise distribution in the eye diagram levels causing BER degradation.

In 3PEAT, the BER will be used to assess the physical layer performance of a link using the project prototype switches. Possible link degradations introduced by the 3PEAT prototypes will be quantified in the form of power overhead, i.e. additional power needed at the receiver side after introduction of the switch in the link in order to achieve the same BER level. A target BER of 10^{-12} will be targeted, being a widely used performance level for commercial systems that is also realistic for a research prototype. The BER will be measured by test and measurement equipment or FPGAs that will be configured to generate test data for testing the 3PEAT link. The FPGAs will be configured with the capability of injecting a PRBS pattern to the system at the transmitter side and measuring the errors at the receiver side after propagation in the 3PEAT DCN network. BER will be evaluated over the payload bits of a test frame, excluding the preamble bits used for locking the clock and data recovery front-end at the receiver.

2.1.1.2 3PEAT testing methodologies

ICCS/NTUA has developed testing methodologies and testbeds for the experimental evaluation and the characterization of the switching modules and more specifically the Module-1 as the first fabricated 3PEAT switching module. These methodologies consist of two main categories. The first one is the static characterization and the functionality evaluation which will be based on the benchtop tests and the second one is the system performance assessment which will be based on the systems test in lab environments.

Regarding the static characterization of Module-1, two different testbeds has been developed. The first one is going to be used for the functionality assessment and consist of a continuous wave light source, the 4x4 switch (Module-1) and an optical spectrum analyzer (OSA) as it is presented in figure 3. Every output of the switch will be connected to the OSA and thus a cross-check of the operating wavelength which travels through every possible optical link inside Module-1 will be made.

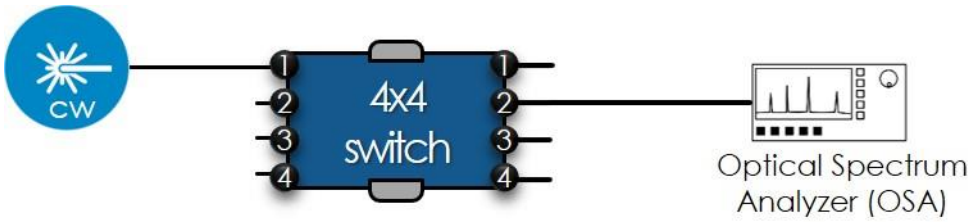

Figure 3: Testbed for the functionality assessment.

The second testbed that corresponds to the static characterization of Module-1, will be used for the reconfiguration time measurement. Figure 4 presents the corresponding setup that incorporates a continuous wave light source, Module-1, a photodiode (PD) and a real

time oscilloscope. By feeding every time, different input of the module, we will measure the light of each output port after passing through the corresponding photodiode at the real time oscilloscope. In this way, the rise and the fall time of each channel will be defined.

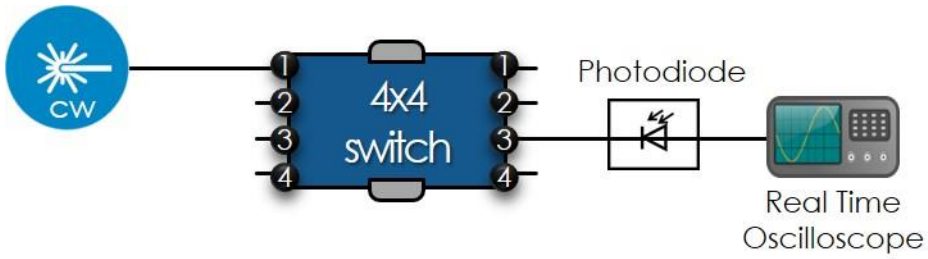

Figure 4: Testbed for the reconfiguration time measurement.

The second category of the testbeds which relies on the system testing of Module-1 in laboratory environments, consists of three different setups.

The first one, which is presented in figure 5, corresponds to the testbed that will evaluate the optical link. This setup comprises a distributed feedback laser (DFB) as a light source, a polarization controller (PC), a pulse pattern generator (PPG) which modulates the Mach-Zehnder modulator (MZM), an Erbium doped fiber amplifier (EDFA) in order to amplify the output light from the tested module, an optical bandpass filter (OBPF) which will filter out the unwanted spectrum, a PD in order to convert the light to an electrical signal and then, a real time oscilloscope (RTO) for the detection of the corresponding signal together with the digital signal processing (DSP) algorithms that will be applied on.

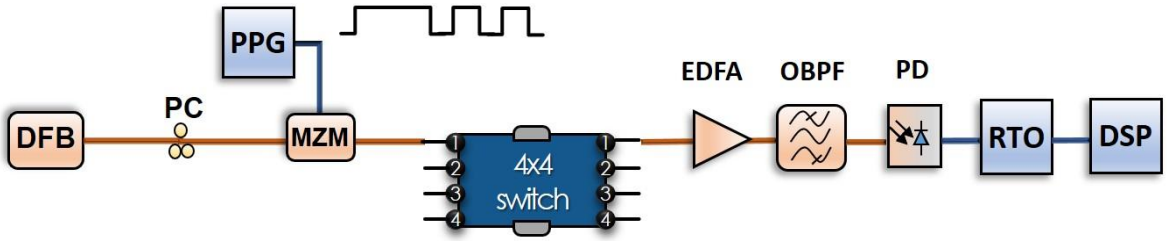

Figure 5: Testbed for the optical link evaluation.

The DSP toolkit relies on a low pass filter (LPF), a time recovery module, an amplitude level control (ALC) and a least mean square (LMS) equalizer before having the symbol detection. This toolkit constitutes the second setup that ICCS/NTUA have developed for the system testing of Module-1 and is being presented in figure 6.

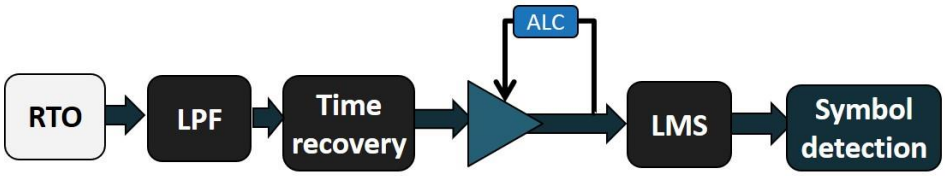

Figure 6: DSP toolkit.

The last setup that has been developed in ICCS/NTUA premises is being presented in figure 7 and is used for the reconfiguration time measurement. In more detail, it is similar to the setup for the optical link evaluation but this time, after the PD, a bit error rate (BER) tester is placed which also feeds the PPG with a clock in order to measure the ratio of the wrong bits received to the total number of bits sent, a procedure which is an essential characteristic that allows to quickly evaluate the quality of the Module-1 link.

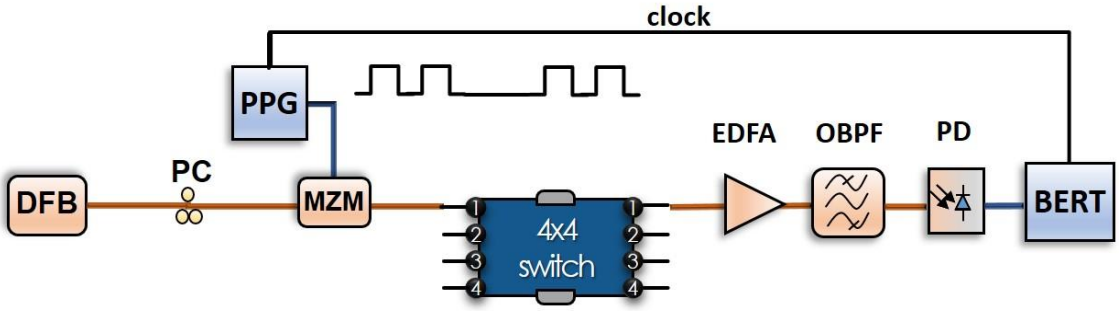

Figure 7: Setup for the reconfiguration time measurement.

2.1.2 Identification of evaluation scenarios

A preliminary specification of the evaluation scenarios for the 3PEAT prototypes has been defined, taking into account the following considerations:

- 3PEAT reference architectures, as reported in internal project reports (deliverable D2.1)
- target specifications of 3PEAT switching modules
- availability of optical (e.g. tunable lasers) and electronic (e.g. FPGAs, broadband amplifiers) components

A small-scale optical DCN will be implemented using the 3PEAT switches to verify the project's technology readiness. The 3PEAT optical DCN will be evaluated in different configurations with increasing integration of the optical switches with networking equipment.

2.1.2.1 3PEAT DCN operation with test measurement equipment

In the initial system experiments, the 3PEAT switches will be integrated into an experimental setup based on state-of-the-art test and measurement equipment. The testbed of ICCS/NTUA will be used for this set of measurements, extending on the basic switch characterization tests described in the previous section. The target test regime is illustrated in Figure 8. A pulse/pattern generator (PPG) will be configured to produce packet traffic, consisting of a pseudo-random binary sequence (PRBS). The data packets will be introduced to a custom-made electro-optic (EO) transmitter based on an externally-modulated laser (e.g. a DFB laser followed by a Mach-Zehnder modulator). This configuration offers flexibility in the evaluation of the device under test, as it allows for deployment of a wavelength-stabilized DFB (as needed for testing of 3PEAT Module 1 and 3) or a fast tunable laser (as required for testing of 3PEAT Module 2). The generated optical packets will be introduced to the optical switch under test, and will be switched to different switch output ports according to an electrical pulse sequence controlling the switch. Two of the optical outputs will be monitored using high speed DC-coupled photodetectors. The optical switch will be controlled by a pulse generator synchronized with the data generating PPG. The pulse generator will produce TTL signals that will drive the 3PEAT electronic control units attached to the optical switch hardware.

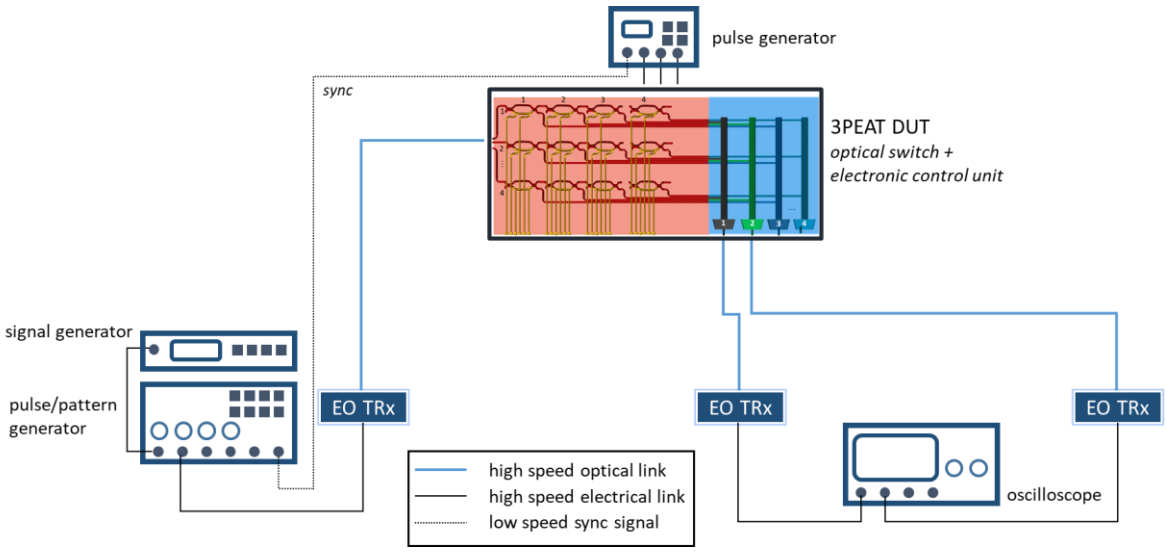

Figure 8: 3PEAT DCN operation with test and measurement equipment.

2.1.2.2 3PEAT DCN operation with networking equipment

In this stage, the 3PEAT switches will be integrated with networking equipment in order to demonstrate successful operation of the optical switch prototypes with commercial end

hosts. The experimental setup of Figure 8 will be upgraded by replacing the test and measurement equipment connected to the electro-optic transceivers with FPGAs or commercial Mellanox network interface cards (NICs). The FPGAs/NICs will be attached to end hosts (servers) generating traffic according to a pre-selected traffic profile. The optical switches will be controlled by an FPGA whereas a custom solution will be developed for synchronizing the server-attached transceivers with the switches so as to enable slotted operation. The setup for this evaluation scenario is depicted in Figure 9.

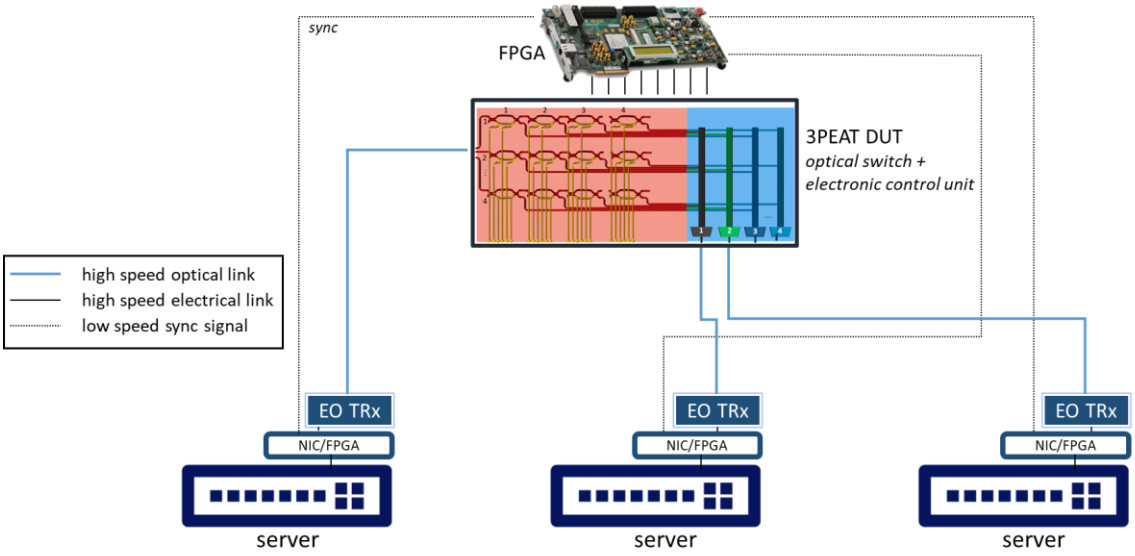

Figure 9: 3PEAT DCN operation with networking equipment.

2.2 3PEAT LDV technology

2.2.1 Definition of testing methodologies (ICCS/NTUA)

Within 3PEAT, possible application scenarios for the three modules have been identified and the corresponding algorithms (i.e. three different modulation schemes) have been developed and described in detail in the internal reports deliverable D2.1 and D2.2.

For the evaluation of these three different algorithms and thus the evaluation of Module-4, two different experimental setups are being developed in ICCS/NTUA premises in collaboration with Optagon.

The first experimental setup, which is presented in figure 10, is based on free-space elements. As a light source, a HeNe laser at 632 nm will be used. After that, an optical isolator will be used in order to avoid any reflections which might deteriorate laser performance. Furthermore, the setup will consist of a combination of free-space elements

(beam splitters, mirrors, polarization converters and polarization beam splitters) forming a Mach-Zehnder-Interferometer. An additional Bragg-cell, which will modulate the "measurement" beam at 40 MHz, will make the setup heterodyne and allow high sensitivity.

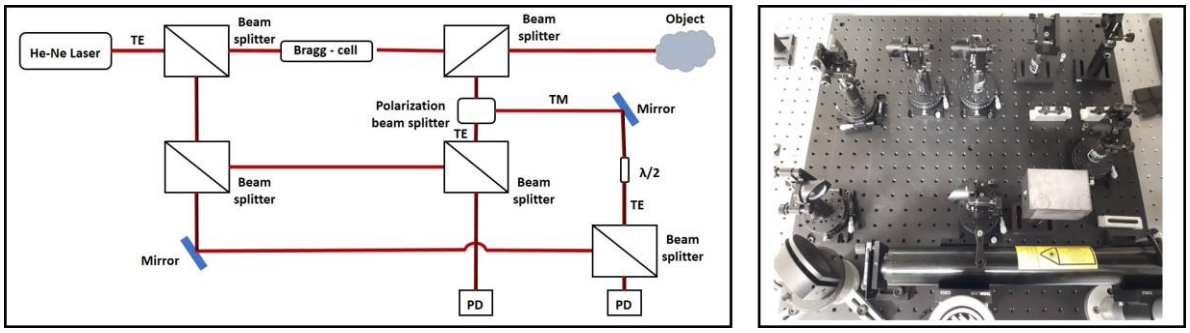

Figure 10: Theoretical scheme of the LDV setup (left), and development of the free-space-based experimental setup (right).

A second, similar experimental setup, operating at 1550 nm, will be based on fiber pigtailed elements and is under preparation at ICCS/NTUA premises.

A further research focus of 3PEAT is the optical phased array (OPA) technology which will be applied in the final LDV module (Module-6). Module-6 will allow the formation of a 2D matrix of light emitting optical antennas and thus will be able to facilitate laser beam scanning both in horizontal and vertical direction.

In order to evaluate the electronics designed by Optagon and to characterize the test OPA structures fabricated by FhG-HHI, an experimental setup has been prepared by ICCS/NTUA and Optagon. Figure 11 presents the layout of this setup based on a probe station where the alignment between an input optical fiber and the PolyBoard test chip can be done. The setup furthermore comprises an external light source at 1550 nm, a polarization rotator and a variable optical attenuator (VOA), a properly designed target surface and an IR camera for tracking the beam on this surface during the beam scanning process. For beam scanning, the algorithms for image processing and the electronics for the adjustment of the phase shifters developed during 3PEAT will be used.

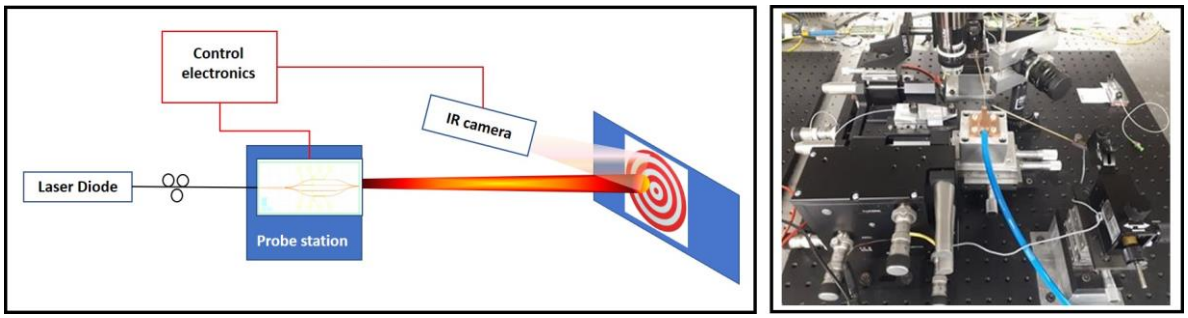

Figure 11: Theoretical design of the experimental setup for the characterization of the OPA test structures (left) and the experimental setup under preparation by ICCS/NTUA and Optagon (right).

2.2.2 Definition of testing methodologies (Polytec)

The definition of testing methodologies need to ensure that the performance of all individual building blocks on the hybrid chip are revealed in detail. This is especially important for module 4, as the findings will serve as a starting point for the elaboration of the subsequent modules 5 and 6. For the more complex modules 5 and 6 the overall performance will be a major focus. Based on the LDV system architecture, as reported in the internal project report deliverable D2.1, the testing procedures at Polytec will include:

- Evaluation of all accessible components on TriPleX- and on Polyboard parts of the hybrid photonic chip.
- Evaluation of all integrated interferometers and photodiodes.
- Evaluation of OPA and beam steering performance of module 6.
- Evaluation in application near test-beds and environments.

Starting point for the definition of evaluation schemes and performance evaluation criteria are the application requirements and demands. State of the art heterodyne LDV technology does reach high sensitivities where even nano Watts of signal light are sufficient for a reliable vibration analysis, and an integrated solution needs to be competitive here. However, the surface characteristics of DUTs may vary from mirror polished metal to rough, black surfaces with pronounced scattering and absorption. Thus, it is of uttermost importance to collect as much as possible signal light and to avoid unnecessary losses on its way to the detector. Following this considerations a first focus during the assessment of the PIC functionality will include all kinds of losses from in- and outcoupling up to excess losses.

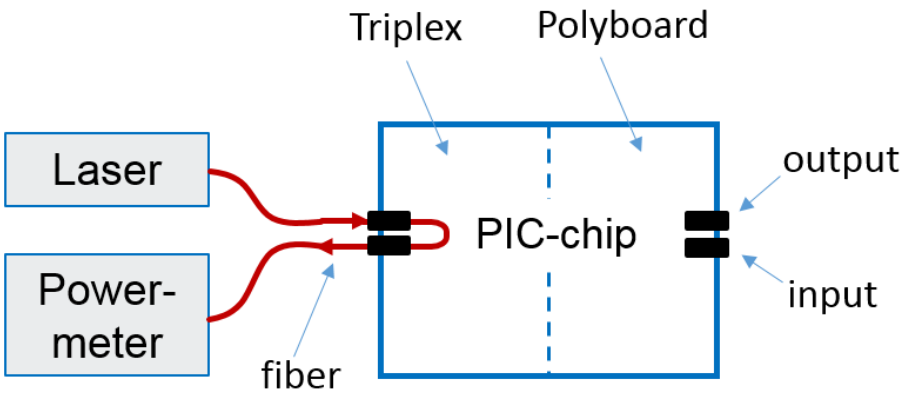

Figure 12: Example of basic set-up to evaluate the PIC chip performance regarding losses.

Figure 12 shows a first basic test scheme of a 3PEAT LDV module to determine in- and out-coupling losses to and from the chip via SM fiber. In the same manner, the performance of integrated splitters and combiners (i.e. partition ratio, leakage) will be accessed and tested. In a next step, the overall throughput through the hybrid chip will be tested to examine

excess losses. Especially the transition losses from TriPleX to PolyBoard are of interest here. Beside the more or less apparent losses, it is necessary to identify and quantify possible crosstalk between optical waveguides and effects of residual carrier light. Such effects inevitably lead to higher noise levels and deteriorate amplitude resolution and vibrational spectra.

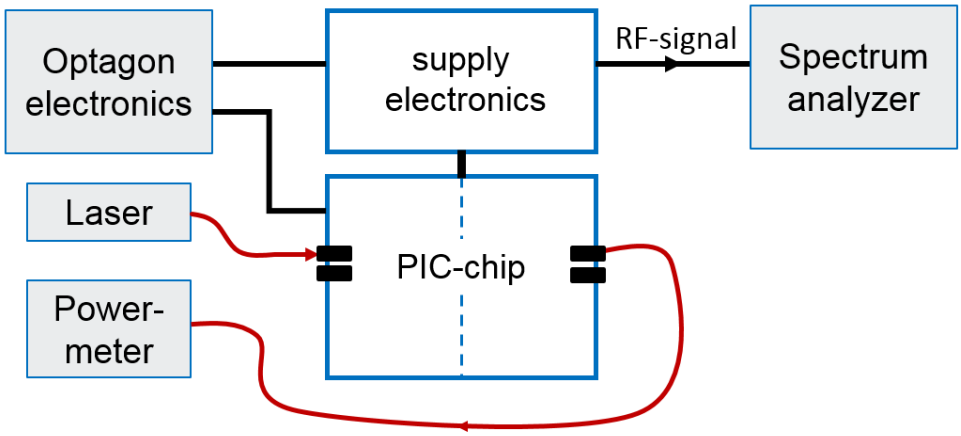

Figure 13: Example of basic set-up to evaluate the overall performances of TriPleX and PolyBoard part.

To gain access to this next higher complexity level additional test equipment like spectrum analyzers and signal demodulation electronics will be used. First of all the performance of the phase shifters will be evaluated related to efficiency, stability and higher order harmonics generation. A schematic test-bed is depicted in figure 13. A defined carrier signal from a state of the art AOM device will be used as reference for performance comparison.

After all individual integrated optical building blocks are evaluated, their interaction as a hybrid chip modules will be tested as a whole. For the control and supply of all PIC functionalities a tailored supply electronics has been developed. A dedicated controller developed by the partner Optagon will drive the assembly. The raw RF signal will be processed and demodulated using an adapted decoder and data management system of Polytec as outlined as example in figure 14. At first, signal out- and input will be short circuited for testing purposes. In a further step a synthetic vibrational signal, generated e.g. via a fiber coupled modulator, will be feed in. This will also allow to evaluate the performance of the subsequent signal processing devices and the interaction of Polytec and Optagon parts.

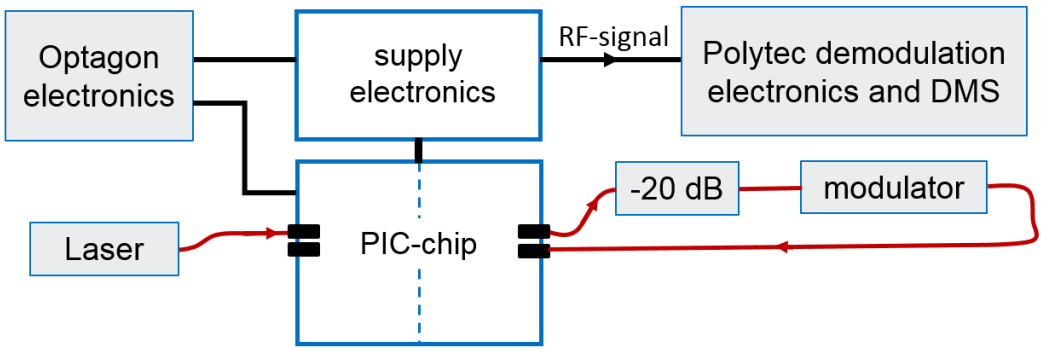

Figure 14: Test-bed example to evaluate the overall performance of the hybrid chip. Introducing e.g. a "synthetic" Doppler shifted signal via an external optical modulator.

Regarding the above outlined testing procedures the following evaluation criteria can be deduced and will be assessed during the system tests:

- Losses
- Crosstalk
- Performance of splitter and combiners
- Performance of photodiodes
- Spurious lines and higher harmonics generation/Influence of residual carrier
- Sensitivity and velocity range of the overall system

2.2.3 Identification of evaluation scenarios

To ensure a successful project implementation, the following prerequisites served as a starting point for the identification of appropriate evaluation and application scenarios:

- The LDV applications should allow a sound evaluation of the performance of the three modules and their individual building blocks.
- A one-to-one comparison with established LDV-technology should be possible.
- The application scenarios should reflect relevant LDV-market environments.

Restricting to medium range applications and based on the uses cases defined in WP2, the typical place and scope of system installation during 3PEAT at Polytec is summarized in table 1.

Place and scope of system installation	Indoor environment intended for industrial R&D-testing.
Material of the surfaces	Rough or smooth surfaces (e.g. polished metal)
Type of characterization	“out-of-plane” motion, single point or scanning.
Distances between LDV and surfaces	1 m – 10 m.

Table 1: Typical place and scope of LDV system installation during 3PEAT.

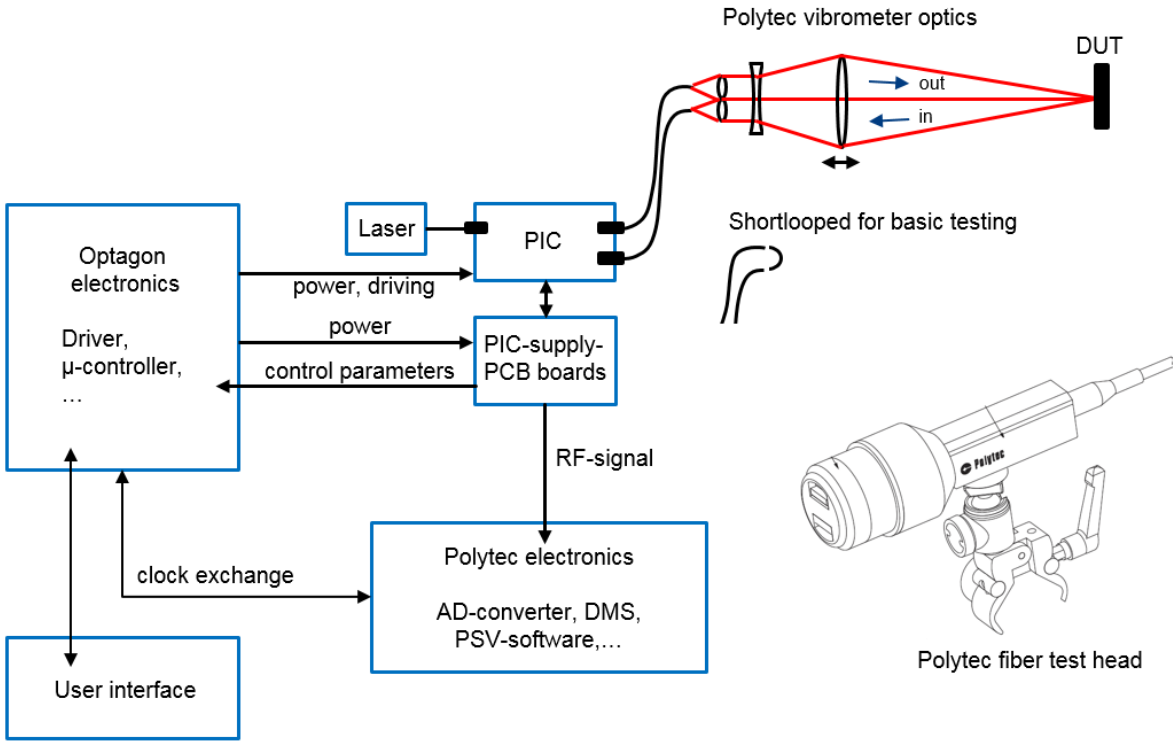

Figure 15: Sketch of the basic set-up for performance evaluation of the 3PEAT LDV modules 4 and 5. The inset on the upper right shows a possible solution for the fibre to free space coupling.

For system tests in application near environments, a concept for light coupling from and to the chip (modules 4 and 5) using additional optics is necessary. The basic concept is outlined in figure 15. To ensure fibre to free space coupling as well as a separation of outgoing and incoming light to the PIC-chip, a fibre based test head from Polytec will be used. The test head will also allow a manual adjustment of the optical focus. In case of module 6, the integrated OPA will be used for in- and out-coupling instead of the Polytec fibre test head.

However, depending on the final design of module 6, Polytec will develop the corresponding necessary free space optics in the next project step.

3. Development of electronic control units

Within WP6, the partners will develop the electronic controllers necessary to drive the 3PEAT modules. The following chapters will highlight the corresponding progress.

3.1 Development of electronic controller and SDO agent for Module-1

Optagon has defined the overall design of the electronic unit for the testing of Module-1, which will be further expanded in order to accommodate the testing of Module-3 in the last part of the project. The unit consists of two main parts, the digital part and the analog part. More specifically, the digital part is based on a Zynq-7000 system on chip (SoC) from Xilinx. The evaluation board of this SoC has the proper number of output ports in order to drive the PZT-based phase shifters that will be present in Module-1. Given the change in the architecture of Module-1 (from the original serial topology to the final tree-topology), the total number of Mach-Zehnder interferometers (MZIs) in Module-1 will be 12. Since each MZI will be equipped with 2 PZT-based phase shifters in order to apply a push-pull scheme, the total number of phase shifters that should be facilitated is 24.

There are two possible schemes for operating these 24 phase shifters. In the first scheme, each phase shifter will correspond to a separate channel and will be operated independently from all other channels. For each channel, the SoC will generate a logic (single-ended) signal with two possible states (i.e. the OFF state corresponding to 0 V and the ON state corresponding to ~2 V). The switching time between the two states will be less than 1 μs in accordance with the system specifications that have been defined in D2.1 and D2.2. After its generation, each signal will be forwarded to the analog part of the unit for processing and amplification in order to drive the phase shifter. In more detail, each signal will be brought/biased symmetrically around 0 V, and will be amplified by a cascade of amplifiers in order to obtain a high peak-to-peak voltage (up to 28 V). Subsequently, for each amplified signal a proper DC level will be added in order to appropriately bias each signal and apply the push-pull signal. Taking as example the case, where the required voltage for pi-phase shift is 20 V (Vpi = 20V), the bias voltage for the phase shifter in the upper branch (PUSH) will be 15 V, while the bias voltage in the lower branch (PULL) will be 5 V. For both signals, the required peak-to-peak voltage is Vpi/2 (10 V). The implementation of this scheme is shown in Figure 16.

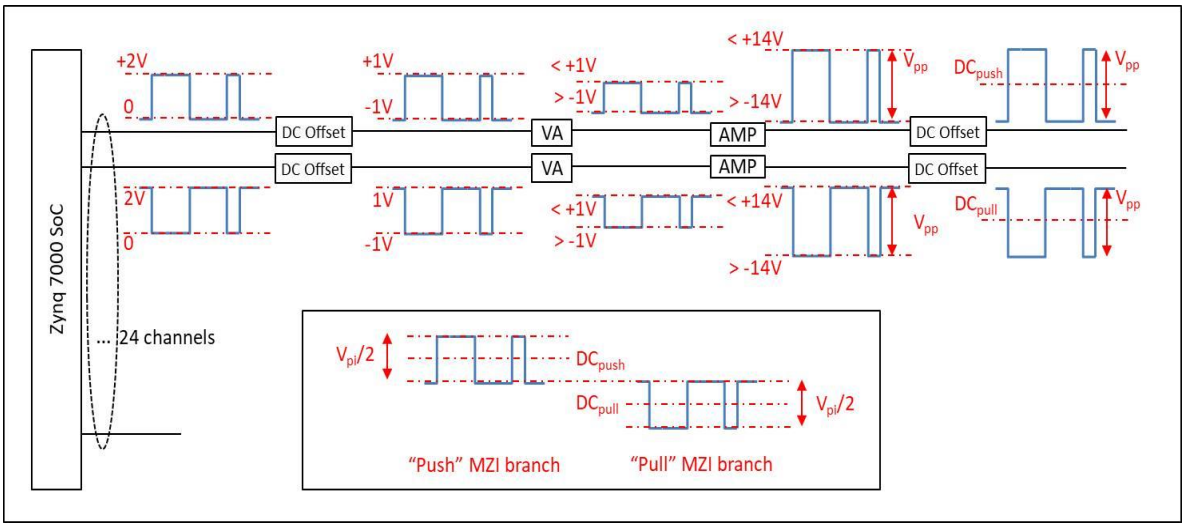

Figure 16: General architecture of the electronic controller for the configuration and testing of Module-1 using a push-pull scheme and independent channels for each one of the PZT-based phase shifters. The inset presents the basic idea/configuration for the operation of an MZI using a push-pull scheme. Given the use of this scheme, the requirement for the Vpp drops from Vpi down to Vpi/2, which may allow the omission of the first DC offset stage.

In the second scheme, the architecture takes advantage of the interdependence of the driving signals due to the use of the push-pull scheme. More specifically, for each MZI, we need only one independent signal (e.g. for the PUSH branch) since the other one (i.e. in the PULL branch) will be always the complementary of the first one. In this case, the number of the independent channels/signals will be only 12, but additional elements are required in the analog part of the unit in order to make this conversion and create the complementary waveform of the PUSH signal for the PULL branch.

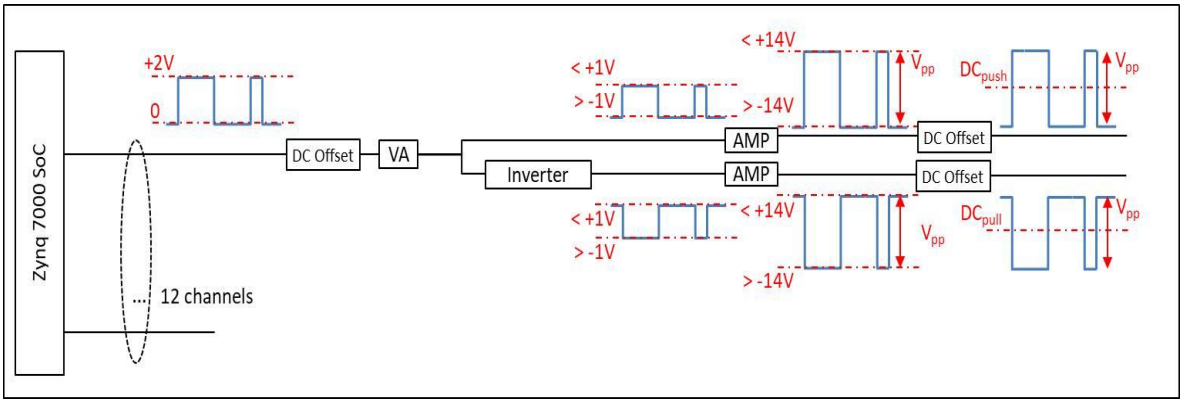

Figure 17: General architecture of the electronic controller for the configuration and testing of Module-1 using a push-pull scheme and interdependent channels for the PZT-based phase shifters inside each MZI. The number of the output ports of the Zynq 7000 SoC that are employed are only half of the PZT-based phase shifters.

3.2 Development of electronic controller for all LDV modules (Module-4-6)

Optagon is also working on the design of the electronic unit that will be responsible for the operation of the LDV modules of 3PEAT. This unit will be responsible for the generation of both low-speed and high-speed signals. The low-speed signals (on the order of kHz) will be responsible for the control of the thermal phase shifters that will be used for the biasing of the couplers in Module-4, and additionally for the control of the micro-ring resonators (MRRs) that will be used inside the cavity of the narrow-linewidth laser in Module-5 and Module-6. Low-speed signals will be additionally used for the control of the PZT-based phase shifters of the optical phase arrays (OPAs) in Module-6. The total number of the thermal phase shifters that will be required in the different versions of Module-4 will be up to 5, whereas the total number of thermal phase shifters that will be required for the operation of Module-5 and Module-6 will be less than 16 (design of Module-5 and Module-6 has not been finalized yet). The total number of the low-speed PZT-based phase shifters is not known yet, and will depend on the yield and the feasible scale of integration that will be achieved both with respect to the number of the parallel layers in the PolyBoard part and the number of the PZT actuators in the TriPleX part. In order to be on the safe side for all these cases, Optagon has been working on the development of a common platform that will be able to operate (using a common graphical user interface) a total number of 16 thermal phase shifters and a number of 32 PZT-phase shifters, expandable to multiples of 32). The digital part of this unit will be based on a Raspberry Pi 3 microcontroller, whereas the analog part will be based on two different sections, one for the thermal phase shifters and one for the low-speed PZT-based phase shifters.

The high-speed signals on the other hand will be responsible for the driving of the serrodyne shifters that are responsible for the modulation and the frequency shift of the generated input, continuous wave (cw) signal. Using as example the Module-4, three versions of the serrodyne shifter have been designed. The first one is based on a simple PZT-based phase shifter (with a single PZT-based phase shifter), which is driven by a single sawtooth wave. The second one is based on a 4-branch serrodyne shifter (with 4 PZT-based phase shifters), which requires 4 sinusoidal signals with pi/2 phase difference between adjacent branches. Finally, the third version is based on what it is internally called as sophisticated serrodyne shifter (with 6 PZT-based phase shifters). In all cases, the electronic control unit should also provide a clock at the operation rate in order to allow for the synchronization of the receiver.

In order to accommodate these needs, the digital part of the control unit will be based on the combination of the Zynq-7000 SoC from Xilinx with a 4-channel DAC from Texas Instruments with 1.5 Gsa/s. The analog part of the unit will be very similar to the

corresponding part of the Module-1 with an amplification chain and possibility for peak-to-peak voltage up to 26 V_{pp}. The first version of the electronics will be designed for operation (frequency shift) at 2.5 MHz. Extension to 40 MHz will be the focus of the next iteration

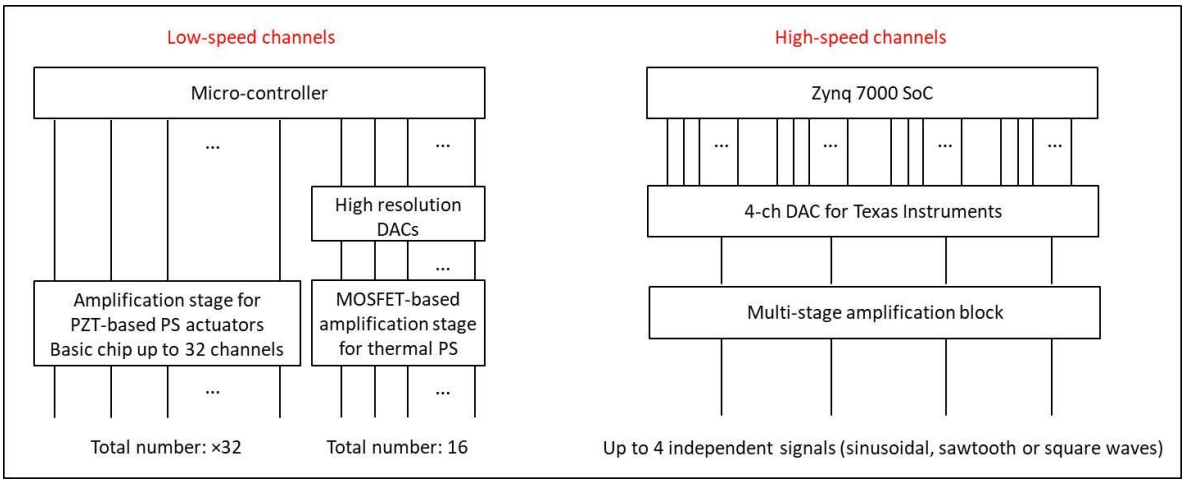

Figure 18: General architecture of the two electronic controllers for the operation of the LDV modules of 3PEAT (Module-4, Module-5 and Module-6).

Beside the control of all integrated optical building blocks of the hybrid chip, which is at the heart of the Optagon controller, an electronic solution for signal processing comparable to state of the art LDV technology is necessary. This part of Polytec's project contribution is split into two parts. First, an adequate solution for signal amplification directly after the detector needs to be developed. Secondly, an adaption of existing demodulation electronics to the demands of the three modules regarding the interaction with the Optagon electronics (e.g. clock exchange) and the packaging requirements is necessary.

Figure 19 depicts the realized supply PCB boards. The two supply boards will be directly attached to the PIC chip using wire bonds and be mechanically mounted to the same base plate. The PCB boards ensure voltage and power supply for the integrated components (detectors, splitters, phase shifters) and are necessary to enhance the expected weak heterodyne signal. The developed electronics will also secure a shot noise limited performance of the interferometer. The signal will be available using standard SMA-cable via additional adapter PCB boards. For the subsequent demodulation electronics, Polytec decoder technology serves as starting point. Due to different carrier frequencies, a sound adaptation of existing demodulation electronics regarding clock exchange between Optagon and Polytec electronics is essential to achieve offset free velocity measurements.

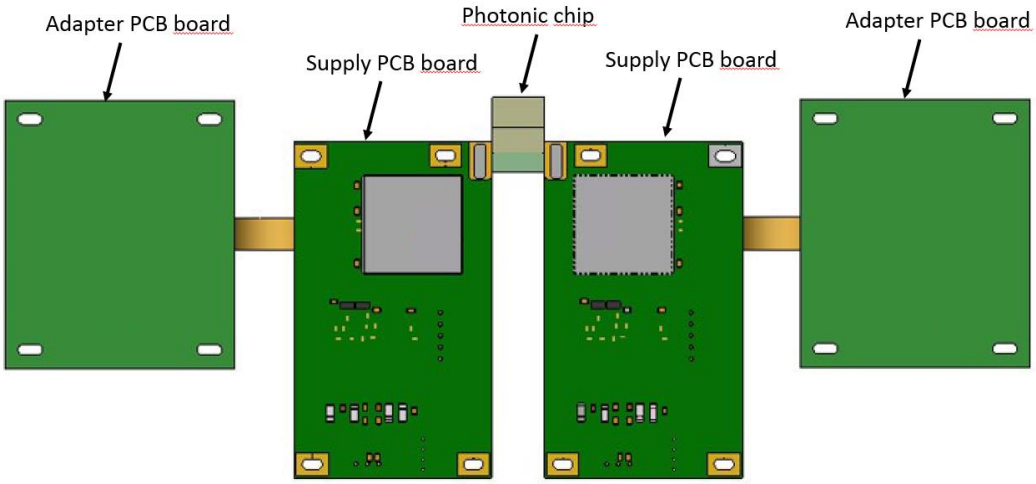

Figure 19: Draft of the PIC supply electronics.

4. Conclusion

ICCS/NTUA in collaboration with Optagon have been prepared and developed different kind of experimental setups for each 3PEAT activity (switches, LDV and OPA). Regarding the evaluation and the characterization of the switching modules, two different setups have been developed to assess the functionality and for reconfiguration time measurements as part of static characterization. For the overall system performance evaluation, three setups have been prepared, one for the optical link evaluation, one DSP toolkit and one for the reconfiguration time measurements in lab environment.

For the LDV and the OPA activities, three different setups are being developed. The first two corresponds to free space-based and a fiber pigtailed-based elements. Both setups will be used for the evaluation of the developed algorithms for the three different modulation schemes. The third one will be used for the characterization of the OPA test chips together with the evaluation of the control electronics, developed from Optagon.

In addition, Mellanox and Polytec have prepared additional lab settings to assess the basic functionalities of the different switching and LDV modules. The testing methodologies have been defined according to the high-level specifications from WP2. Furthermore, application near test beds have been developed to evaluate the device performance.

The partners also developed the necessary electronics to drive the switching and LDV module.

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